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10/755,608	01/12/2004	John L. Schantz	200309943-1	9939

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
ARCOS, CAROLINE H	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/755,608	SCHANTZ, JOHN L.	
	Examiner	Art Unit	
	Caroline Arcos	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/12/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 are pending.

Claim Objections

2. Claims 2 is objected under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1 is rejected under 35 U.S.C 101 because it is both system and method claim which is directed to non- statutory subject matter. Claims 1 should be a method claim or a system claim; examiner interprets claims 1 as a method claim because all dependant claims are method claims.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being a method and a system claim. Claims 1 should be a method claim or a system claim; examiner interprets claims 1 as a method claim because all dependant claims are method claims.
6. Claims 3 is rejected under 35 U.S.C. 112, second paragraph, as being unclear and indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
7. Claim 3 points out if in a second scenario alternative to said first scenario, said utilization level of said one of said processors exceeds said average utilization level by more than said predefined threshold, incrementing said load value assigned to each of said plurality of processors, if an immediately preceding adjustment to a load value of a processor in said plurality of processors was a decrement. Claim 3 did not clearly specify that those processors having "increase-decrease" condition would be excluded from being incremented according to figure 5 and the specification. Examiner interprets claim 3 as follow:" if in a second scenario alternative to said first scenario, said utilization level of said one of said processors exceeds said average utilization level by more than said predefined threshold, incrementing said load value assigned to each of said plurality of processors except processors whose preceding adjustment to a load value of said processors was decrement. "

Claim Rejections - 35 USC § 102

8. Claims1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Beaumont (US 2004/0216117 A1).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Per claim1:

- In a computer system, a method for redistributing workload among a plurality of processors (Paragraph 0002, lines 1-4 "The present invention relates generally to parallel processing and more particularly to balancing the work loads of the processing elements within a parallel processing system.") where "elements" within a parallel processing system are plurality of processors as claimed.

- each processor of said plurality of processors being associated with a load value that indicates a level of workload assigned to said each processor (Paragraph 0012, lines 5-6 "each of the plurality of PEs has a local number of tasks associated therewith. ") where "PEs" are plurality of processors as claimed.

- determining an average utilization level for said plurality of processors (Paragraph 0012, lines 9-10" calculating a local mean number of tasks for each of the plurality of PEs") where "mean number of tasks for each of the plurality of PEs" is the average utilization as claimed.

- if a utilization level of one of said processors is above said average utilization level by more than a predefined threshold, incrementing, in a first scenario, said load value assigned to each of said plurality of processors, except processors whose utilization level is

above said average utilization level by more than said predefined threshold and whose immediately preceding adjustment to its load value in a previous adjustment cycle was an increment. Figure 5(a, b, c, d and e) PE1, PE3, PE4 and PE7 their utilization level, which is the number of tasks, is above average utilization level "Mr", increment PE0, PE2, PE5 and PE6 which their utilization level below the average utilization level. Figure 5c shows that PE0 increment and its preceding load value adjustment was incrementing to be balanced with all other PEs as claimed.

Claim 2 is the same as claim 1 and rejected for the same reason.

Per claim3:

Claim 1 is incorporated and further Beaumont Discloses:

If, in a second scenario alternative to said first scenario, said utilization level of said one of said processors exceeds said average utilization level by more than said predefined threshold, incrementing said load value assigned to each of said plurality of processors if an immediately preceding adjustment to a load value of a processor in said plurality of processors was a decrement. Figure 5(a, b, c, d and e) shows PE1, PE3, PE4 and PE7 their utilization level, which is the number of tasks, is above average utilization level "Mr", increment PE0, PE2, PE5 and PE6 which their utilization level below the average utilization level and decrement the load value on PE1, PE3, PE4 and PE7. Figure 5c shows that PE0, PE2 increment and PE4 preceding load value adjustment was a decrement to be balanced with all other PEs as claimed.

Per claim4:

Claim 3 is incorporated and further Beaumont Discloses:

-wherein said incrementing in said second scenario is performed only if there exists a first processor among said plurality of processors whose utilization level, prior to said incrementing, is above said average utilization level by more than said predefined threshold and whose immediately preceding adjustment to a load value of said first processor in said previous adjustment cycle was an increment. Figure 5(a, b, c, d and e) shows PE1 its utilization level, which is the number of tasks, is above average

utilization level "Mr", increment PE0, PE2, PE5 and PE6 which their utilization level below the average utilization level and decrement the load value on PE1, PE3, PE4 and PE7. Figure 5c shows that PE0, PE2 increment and PE4 preceding load value adjustment was a decrement to be balanced with all other PEs as claimed. Whether it is decrease-increase or increase-increase, all processors in the plurality of processors will be incremented except the one that their utilization level is above the average utilization level.

Per claim5:

Claim 3 is incorporated and further Beaumont Discloses:

-adjusting, in a third scenario alternative to both said first scenario and said second scenario, load values associated with selected processors of said plurality of processors, said selected processors including a first group of processors whose utilization level exceeds said average utilization level by more than said predefined threshold and a second group of processors whose utilization level is below said average utilization level by more than said predefined threshold, said adjusting including decrementing load values associated with said first group processors and incrementing load values associated with said second group of processors. Figure 5(a, b, c, d and e) shows PE1, PE3, PE4 and PE7 their utilization level is above average the utilization level, their load value decremented and PE2, PE5 and PE6 which their utilization level is below the average utilization level, their load value is increased as claimed.

Per claim6:

Claim 1 is incorporated and further Beaumont Discloses:

-incrementing said load value associated with said each of said plurality of processors. if a bundle value of any of said plurality of processors is below a minimum bundle value. Figure 5(a, b, c, d and e) shows PE2 task number, which is bundle value, is below minimum bundle value is incremented from value 2 to value 5.

Per claim7:

Claim 1 is incorporated and further Beaumont Discloses:

- said incrementing is accomplished by adding a predefined value to said load value associated with said each of said plurality of processors. Figure 5(a, b, c, d and e) shows that the incrementing is by adding predetermined value "1" each time it increments.

Per claim8:

Claim 7 is incorporated and further Beaumont Discloses:

- a determination of whether said utilization level of said one of said processors, is above said average utilization level by more than said predefined threshold employs a standard deviation calculation. (Paragraph 0012, lines 10-11 "calculating a local deviation for each of the plurality of PEs."), (Paragraph 0052, lines 3-5 " The local deviation is simply the difference between the local value and the local mean (Dr=Vr-Mr"), and ((Paragraph 0053, lines 1-9 " After the local deviation (Dr) are computer in operation 64, a first local cumulative deviation (Lr) for each PE is determined in operation 65…the number tasks (Vr)")

Per claim9:

Claim 8 is incorporated and further Beaumont Discloses:

- said determination of whether said utilization level of said one of said processors is above said average utilization level by more than said predefined threshold is performed without taking into account low priority processes, said low priority processes representing processes whose priority level is below a pre-defined priority level. It is inherent that thread scheduling works on the higher priority tasks; the lower priority tasks are at the bottom of the scheduling queue. They don't get counted into scheduling until the higher priority tasks are completed.

Per claim10:

Claim 1 is incorporated and further Beaumont Discloses:

- said workload is divided into a plurality of bundles, said load level associated with said each processor of said plurality of processors is expressed in bundle units. (Paragraph 0002, lines 1-4 "The present invention relates generally to parallel processing and more particularly to balancing the work loads of the processing elements within a parallel processing system."), and

(Paragraph 0040, lines 1-7 " Fig. 4 illustrates an operational process 60 for balancing the work loads between the PEs 30 in line 50...determining the total number of tasks (V) present in the line operation 61...therewith.")

Per claim11:

Claim 10 is incorporated and further Beaumont Discloses:

- said each of said plurality of processors is assigned an initial bundle value at system startup. (Paragraph 0012, lines 4-5 " each of the plurality of PEs has a local number of tasks associated therewith."), and (Paragraph 0041, lines 4-5" The sum (Sr) is initialized to the number of tasks")

Per claim12:

Claim 1 is incorporated and further Beaumont Discloses:

-said plurality of processors are fewer in number than a total number of processors executing processes in said computer system. (Paragraph 0008, lines 1-15 " parallel processing...The workload of the CPU may be reduced to operating system tasks, such as scheduling processes and allocating system resources") the CPU is divided into PEs that are doing different functionality, some are allocating resources and others are scheduling processes which are fewer than the total number of processors executing the processes.

Per claim13:

Claim 1 is incorporated and further Beaumont Discloses:

- said workload is redistributed periodically throughout an execution lifetime of a given process. (Paragraph 0014, lines 1-3" The present invention enables tasks to be distributed along a group of serially connected PEs so that each PE typically has X number of tasks or (X+1) number of tasks to perform in the next phase.") And (Paragraph 0057, lines 4-5" "the tasks associated with each PE are redistributed among the PEs")

Claims 14- 25 are the article of manufacture claims of the method claims 1-3 and are rejected under same reasons.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

TITLE: Load Balancing Based on Queue Length in a network or processor stations, US 6,128,642

TITLE: Method, system and program products for managing central processing unit resources of a computing environment US 6,587,938 B1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caroline Arcos whose telephone number is 571-270-3160. The examiner can normally be reached on Monday-Thrusday 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Patent Examiner

Caroline Arcos

Caroline Arcos EA

CHAMELI DAS
SUPERVISORY PATENT EXAMINER

9/4/07